AN-478A

Application Note

9004XG071H

SMALL-SIGNAL RF DESIGN WITH DUAL-GATE MOSFETS

Prepared by

Brent Trout

Applications Engineering

The dual-gate MOSFET offers low noise, high gain, and excellent AGC, cross-modulation and overload characteristics in RF applications. Recent devices also feature silicon nitride passivation for ease of handling and reliability. This note discusses the characteristics of dual-gate MOSFETs, with emphasis on circuit design noise figure, AGC, bandwidth and detuning, cross-modulation and mixer operation.

MOTOROLA *Semiconductor Products Inc.*

9004XG-071H

SMALL-SIGNAL RF DESIGN WITH DUAL-GATE MOSFETS

INTRODUCTION

The dual-gate metal-oxide-semiconductor field-effect transistor (MOSFET) is no longer a new development in transistor technology. It has gained widespread acceptance and is currently being designed into RF amplifiers, mixers, demodulators, and other RF applications. A few reasons for its success are high gain, low noise, and excellent AGC, cross-modulation, and overload characteristics.

MOSFET technology was hampered for some time by dc bias-point instability. This bias point drift was due to the gradual migration of sodium contaminants in the gate oxide layer. Motorola has solved this problem with silicon-nitride passivation. In addition to being impervious to sodium ion contamination, the silicon nitride has also yielded higher gate breakdown voltages and greater ruggedness. Maximum ratings for V_{G1S} and V_{G2S}, which were typically ±15 V for older devices, are now ±35 V for the MFE3007. Transient ratings are many times higher. The greater ruggedness of the new silicon-nitride passivated devices will be appreciated by those who are familiar with the delicate handling often required with older devices. The author took no special precautions in his laboratory work with the devices used and no static-charge failures were encountered.

The intent of this application note is to acquaint the designer with the RF capabilities and design data for the dual-gate MOSFET. Although the specific device and performance data presented in this application note are for the MFE3007, the RF circuit design theory and discussions will pertain to the dual-gate MOSFET in general, including diode protected types. The MFE3007 is an N-channel, type-B MOSFET. The type-B designation implies operation in both the enhancement and depletion modes.[1]

DEVICE OPERATION

Figure 1 shows a cross-section of the dual-gate MOSFET. The construction of the dual-gate transistor is similar to that of the single-gate MOSFET, the major difference being the addition of a second gate.

A brief explanation of the device operation will be given for those unfamiliar with the MOSFET. A more detailed analysis is given in Reference 1. Two polarities of MOSFETs are presently being manufactured, N-channel and P-channel. The channel type refers to the type of impurity used to dope the drain-to-source conduction path. For the MFE3007, the free-charge carriers are electrons, hence the N-type designation. For a P-type device, conduction is by "hole" carriers. The "N+" areas under the source and drain of Figure 1 are highly doped N-type regions. That is, they exhibit a high concentration of free electrons. The areas beneath gates 1 and 2, outlined by the dashed lines, are the conduction channels which are much more lightly doped. The conductivity of these channels is controlled by the gate voltages in the following manner: When a positive voltage is applied between a gate and the source, a negative charge is induced in the channel opposite the gate. The induced negative charge increases the free-electron concentration, and therefore the conductivity in that portion of the channel. This is the mechanism by which the output current is modulated by the input gate voltage. The extent to which the output current changes for a small change in the input voltage is given by the transconductance (g_m, y_{fs}, y_{21}) and is a measure of the device's ability to amplify. Since the dual-gate MOSFET is a voltage-controlled device, once the pinch-off voltage is overcome, the output current (I_D) is dependent only on gate voltages. The pinch-off voltage is the drain-to-source voltage (V_{DS}) at which the drain current reaches a limiting value where further increases in V_{DS} do not produce any appreciable increase in the drain current.

Figure 2 shows typical output characteristics for the common-source configuration. The curves are for V_{G2S} = 4 Vdc, which will be shown to be optimum gate-2 bias for most amplifier applications.

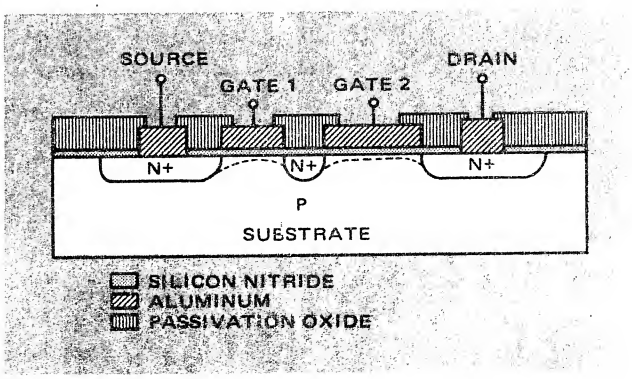


FIGURE 1 – Dual-Gate MOSFET Cross Section

1. For the reader unfamiliar with such terms as "enhancement" and "depletion", a detailed discussion of field-effect transistors is given in Reference 1.

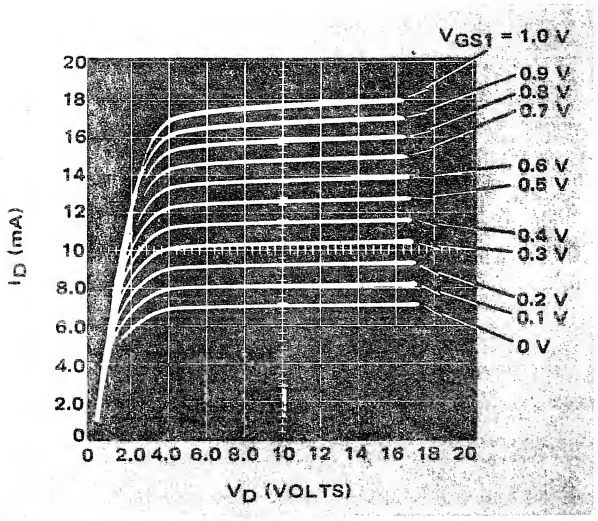


FIGURE 2 – Output Characteristics of MFE3007 at V_{G2S} = 4.0 V

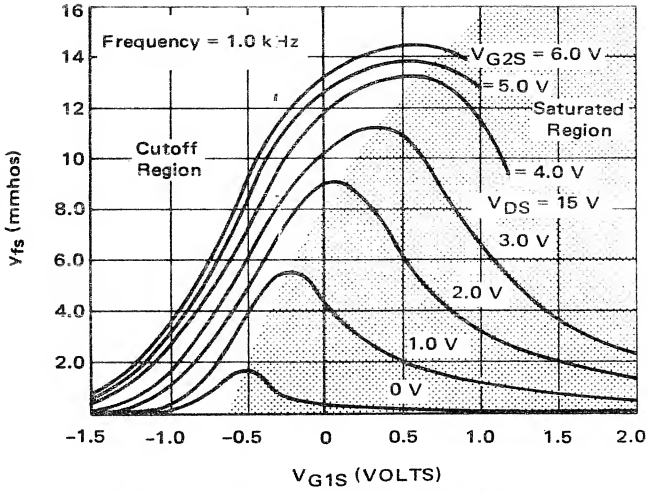


FIGURE 3 – y_{fs1} versus Bias Point of MFE3007 Dual-Gate MOSFET

In theory, either gate can be used for the signal input gate as both exhibit sufficient gate-to-drain transconductance (Figures 3 and 4). However, due to device design and certain practical considerations, gate 1 functions best as the input gate. When gate 2 is used for signal injection, the channel resistance controlled by gate 1 acts as an unbypassed source resistance as shown in Figure 5. Since it is impossible to bypass this degenerative source impedance, the device gain is lowered. Figure 5 also shows an equivalent representation of the device when the signal is injected at gate 1 with gate 2 bypassed to ground for ac. In this mode of operation, the device is equivalent to a common-source common-gate cascode amplifier. The common-gate portion serves as a variable-impedance buffer stage between the input and output. The variable drain resistance in Figure 5 is controlled by the dc voltage applied to gate 2; its value decreases with increasing gate-2-to-source voltage. This configuration is analogous to the common-cathode–common-grid cascode amplifier often employed in vacuum tube circuits for high isolation between input and output. Both the grounded-gate buffer and the physical separation between gate 1 and drain help achieve an extremely high degree of input-output isolation. The feedback capacitance between drain and gate 1, C_{rss}, is typically only 0.02 pF. Unless otherwise stated, all further references to transconductance or amplifier characteristics will assume a common-source configuration with signal injection at gate 1, and gate 2 ac-bypassed to ground.

DESIGN APPROACH

Design of small-signal RF amplifiers using two-port networks has achieved excellent results with FET as well as bipolar-transistor and integrated circuit RF amplifiers. This method is described in detail in references 2 and 3.

Basically, it consists of characterizing the active device as a linear active two-port network (LAN) with admittances (y parameters), and using these parameters to solve exact design equations for stability, gain, and input and output admittances. A y parameter is an expression for admittance in the form

$$y_{is} = g_{is} + jb_{is},$$

where g_{is} is the real (conductive) part of the admittance and b_{is} is the imaginary (susceptive) part. These admittances

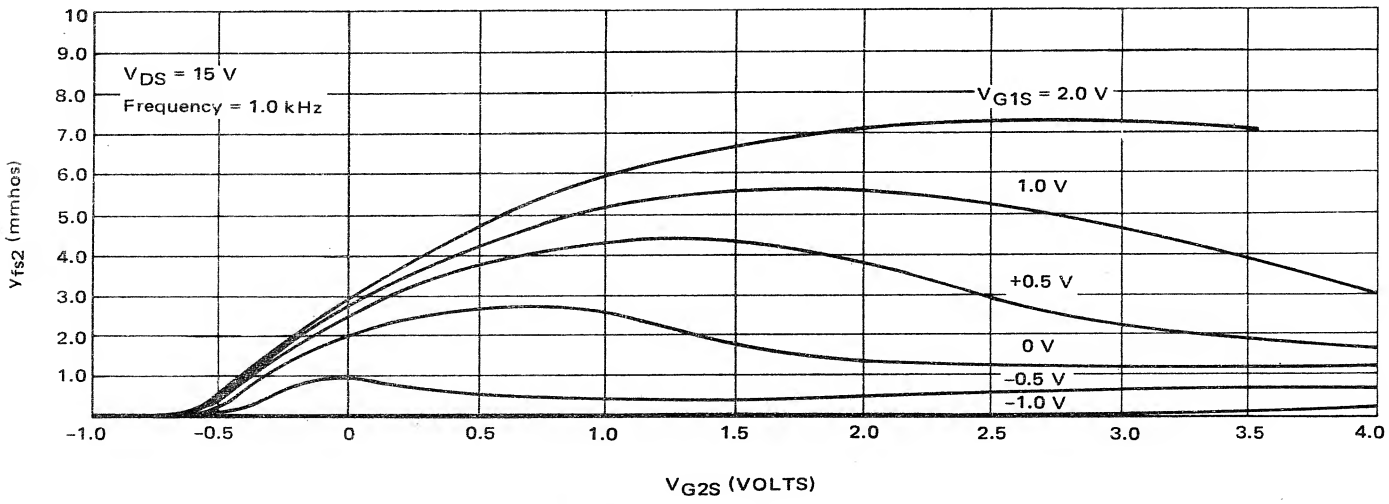


FIGURE 4 – y_{fs2} versus Bias Point

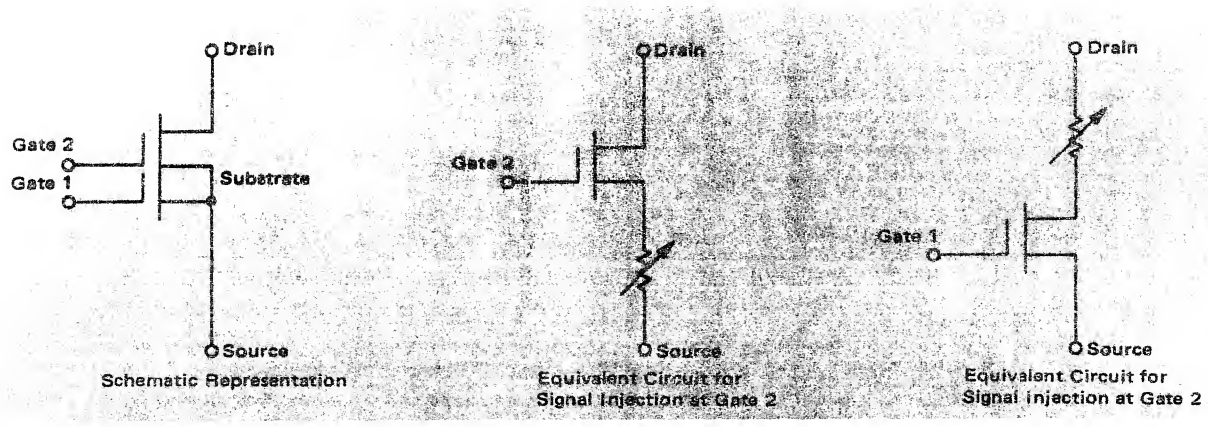


FIGURE 5 – Equivalent Dual-Gate MOSFET Circuits with Signal Injection at Gates 1 and 2

are used instead of the more common impedances (z parameters) because they greatly simplify the measurements and calculations.

Scattering (s) parameters are increasing in popularity and may be used instead of y parameters with appropriate design equations. Since the two port network design method described in this report and the references does not include assumptions or shortcuts, the theoretical design solution will be the same regardless of which parameter set is used.

Equally satisfying results have been achieved using this approach to the design of RF-amplifier circuits using dual-gate MOSFETs.

Y PARAMETERS

Common-source admittance (y) parameters for the MFE3007 are shown in Figures 6 through 9. RF Designers have traditionally used the nomenclature y_{11}, y_{12}, y_{21}, and y_{22} for all active devices – bipolar transistors, integrated circuits, and other devices. However, y parameters for FETs are registered using descriptive lettered subscripts:

y_{is} (input admittance) = y_{11}

y_{rs} (reverse transadmittance) = y_{12}

y_{fs} (forward transadmittance) = y_{21}

y_{os} (output admittance) = y_{22}

The "s" refers to common-source operation. As these lettered symbols appear on data sheets, they are used in this application note. In a dual-gate device, the subscript 1 can be included to indicate admittance between gate 1 and the source, for example, y_{fs1}. As previously noted, the input port is understood to be gate No. 1.

Parameters y_{is}, y_{os}, and y_{fs} were measured on a General Radio Transfer Function and Immittance Bridge. When measuring the extremely low input and output conductances, appropriately high valued carbon resistors were also measured to insure the accuracy of the readings. The dc conditions for all measurements were V_{DS} = 15 V, V_{G2S} = 4 V, and V_{G1S} adjusted for an I_{DS} of 10 mA. Care was taken to provide an effective ac ground at gate 2 since this is especially important in achieving circuit stability in a practical design.

Both the real and imaginary parts of the feedback admittance, y_{rs}, are too small for measurement on the G.R. bridge over the useful frequency range of the device. For all practical purposes, the real part of the feedback admittance can be assumed to be zero. The imaginary part of this admittance was measured at 1 MHz on a Boonton Capacitance Bridge. It is typically 0.02 pF. For admittance values at higher frequencies this capacitance is assumed to be a constant. In a practical design application, however, the effect of parasitic capacitance upon the feedback admittance should be considered. Even in a reasonably well-shielded amplifier, the stray capacitance may turn out to have a value greater than the small feedback capacitance of the dual-gate FET itself. The amplifiers described in this report had total feedback capacitances (device plus stray) of 0.050 to 0.1 pF.

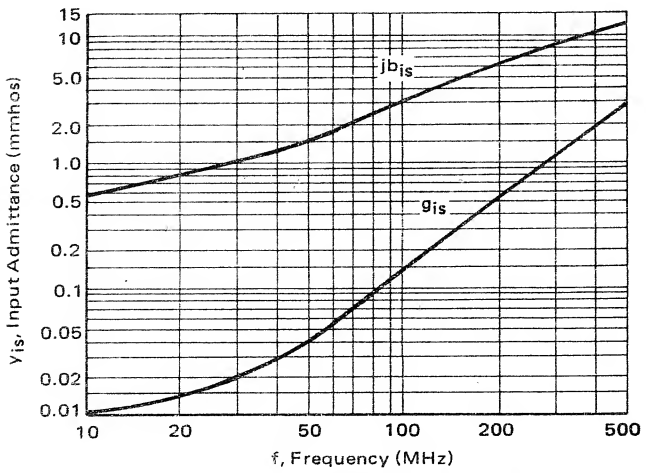


FIGURE 6 – MFE3007 Input Admittance versus Frequency

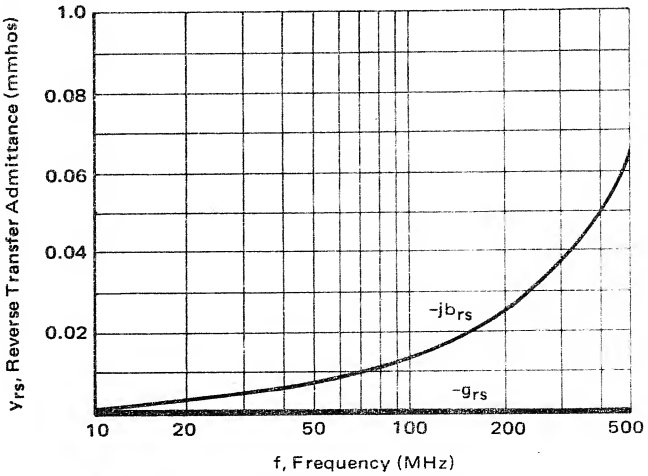


FIGURE 7 – MFE3007 Reverse Transfer Admittance versus Frequency

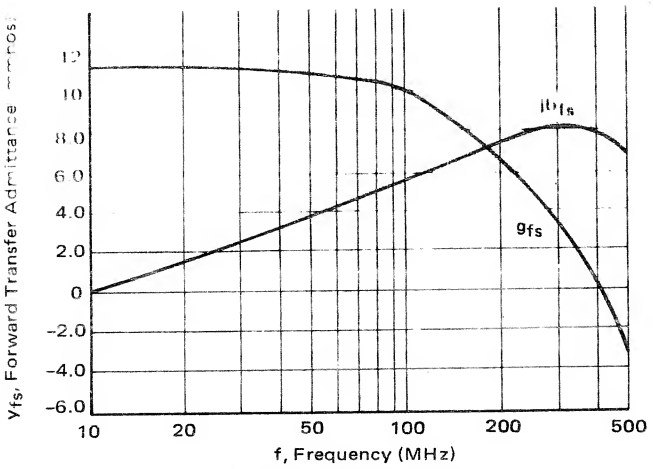


FIGURE 8 – MFE3007 Forward Transfer Admittance versus Frequency

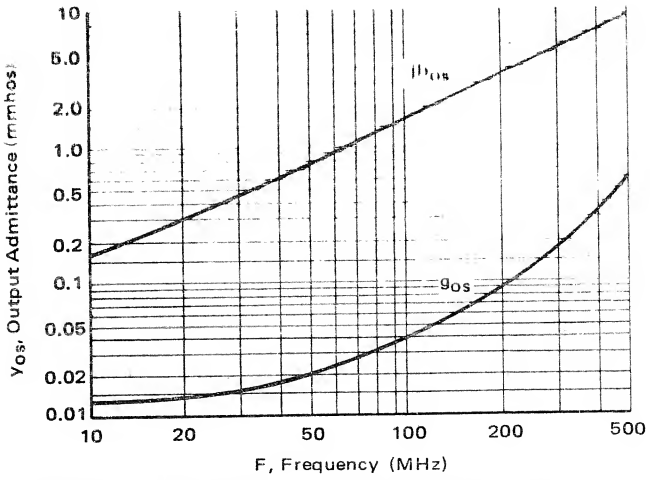


FIGURE 9 – MFE3007 Output Admittance versus Frequency

Admittance parameters for the common-gate configuration were also measured. Although the lower input impedance of the device in this configuration ($g_{is} \approx 12$ mmhos at 50 MHz to 200 MHz) may be advantageous for matching at the input, the attendant reduction in the available power gain renders this type of operation undesirable in most applications. Analyses show the unneutralized power gain of this configuration to be 10 to 15 dB lower than the common-source power gain.

DESIGN DATA

For convenience in designing with the MFE3007, several significant equations have been solved by computer. Their solutions are plotted in Figures 10 through 13. An explanation of these curves is given below. For additional examples of the use of such computer-derived circuit design curves, see reference 4.

The reverse transadmittance used to generate this design data was $0\text{-}j\omega\ (0.1 \cdot 10^{-12})$ mhos, which represents a composite feedback capacitance of 0.1 pF. This value can be obtained in a circuit with careful layout, and is a more practical value than the 0.02 pF feedback capacitance of the device alone.

The Linvill stability factor, C, which is a measure of device open-circuit stability, is plotted in Figure 10. C is greater than 1 below 250 MHz, thus the device is potentially unstable below 250 MHz and unconditionally stable above 250 MHz.

Figure 11 shows transducer power gain for the MFE3007 in both the unilateralized (neutralized) and the unneutralized (no negative feedback) configurations. The higher gain curve represents unilateralized operation. The lower gain curve shows G_{max} (the maximum possible transducer gain without negative feedback) in the unconditionally stable region above 250 MHz.

In the potentially unstable region (below 250 MHz), mismatching must be used to guarantee stability if negative feedback is not used. The design equations were solved for the highest gain per degree of circuit stability. Circuit stability is measured by the Stern circuit stability factor, k, which is discussed in Reference 2.

The portion of the unneutralized gain curve below 250 MHz in Figure 11 represents a circuit stability factor of 3.

To further aid in circuit design with the MFE3007, the design equations to achieve the unneutralized performance shown in Figure 11 for complex source and load admittances

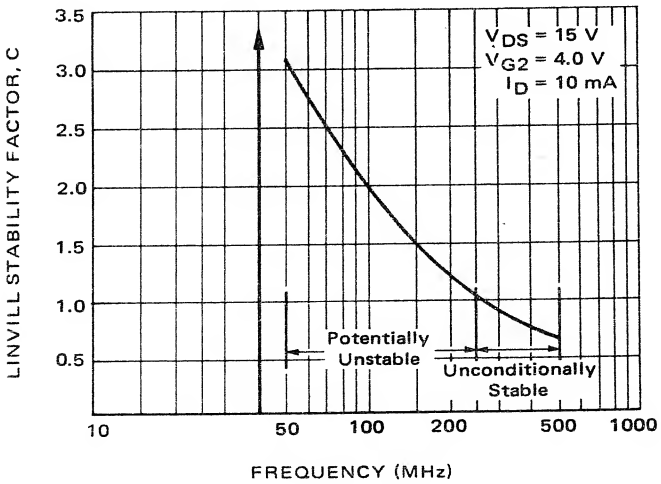


FIGURE 10 – Linvill Stability Factor, C, for the MFE3007 Between 50 and 500 MHz

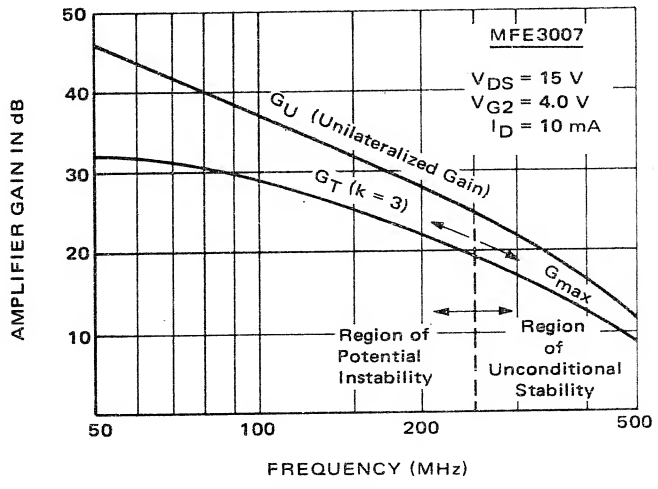


FIGURE 11 – Amplifier Gain Characteristics in Common Source Configuration

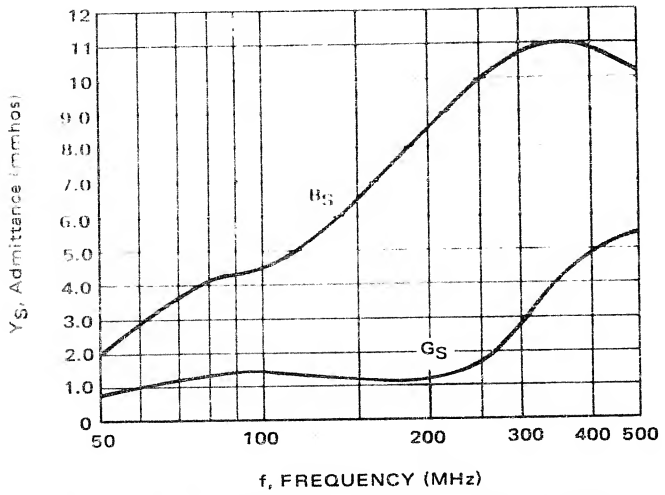


FIGURE 12 – Optimum Source Admittance, $Y_S = G_S + jB_S$, for Unneutralized G_T of Figure 11

have also been solved by computer. The results are given in Figure 12 and 13. Thus the design of an unneutralized amplifier may be greatly simplified by first checking Figure 11 to determine the expected gain and then obtaining the optimum device complex source and load admittances from Figures 12 and 13. The only remaining step would then be network synthesis to calculate the required source and load admittances at the gate 1 and drain terminals of the FET, as determined above. The peculiar shape of the load and source conductance curves of Figures 12 and 13 can be explained as follows:

As the frequency increases, $|y_{fs}|$ decreases, permitting a closer match of the source conductance (G_S) to g_{is}, and the load conductance (G_L) to g_{os}, while still maintaining the same circuit stability. Since the degree of mismatch is decreasing faster than g_{os} is increasing, the load conductance continuously decreases until the device approaches unconditional stability. For the region above conditional stability (above 250 MHz), both source and load conductances increase, matching the increasing input conductance (G_{IN}) and output conductance (G_{OUT}).

DESIGN PROCEDURE

To demonstrate the use of Figures 10 through 13, the design procedure for a 100-MHz common-source amplifier will be discussed. The circuit is shown in Figure 14. From Figure 10, the Linvill stability factor C is seen to be 2.0, therefore mismatching or neutralization is necessary to prevent oscillation. Mismatching will be used in this example. Figure 11 shows that for a circuit stability factor of 3.0, the transducer gain will be 28 dB. The load and source admittances for the required mismatch and gain are found from Figures 12 and 13:

$$Y_L = 0.35 - j2.1 \text{ mmhos},$$
$$Y_S = 1.3 - j4.4 \text{ mmhos}.$$

At this frequency, y parameters for the MFE3007 are:

$$y_{is} = 0.15 + j3.0$$
$$y_{fs} = 10 - j5.5$$
$$y_{rs} = 0 - j0.012$$
$$y_{os} = 0.04 + j1.7$$

Assuming the load and source impedances are both 50 ohms, networks can be designed to match the MOSFET to the load and source. The calculations are more easily performed with impedances rather than admittances. The procedure will first be discussed for the output matching.

The 50-ohm load impedance must be transformed to the optimum load for the transistor ($Y_L = 0.35 - j2.1$). This transformation can be performed by the network shown in Figure 15A. The 50 ohms must be transformed to

$$R_L = \frac{1}{G_L} = \frac{1}{0.35 \times 10^{-3}} = 2.86 \text{ k}\Omega$$

The series capacitive reactance required for this matching can be found by

$$X_{C4} = X_S = R_S\sqrt{\frac{R_P}{R_S} - 1}$$

where R_P is the parallel resistance and
R_S is the series resistance.

$$X_{C4} = 50\sqrt{\frac{2.86 \times 10^3}{50} - 1} = 375\ \Omega$$

The capacitance that provides this reactance at 100 MHz is

$$C4 = \frac{1}{2\pi f X_{C4}} = \frac{1}{2\pi(10^8)(375)} = 4.2 \text{ pF}$$

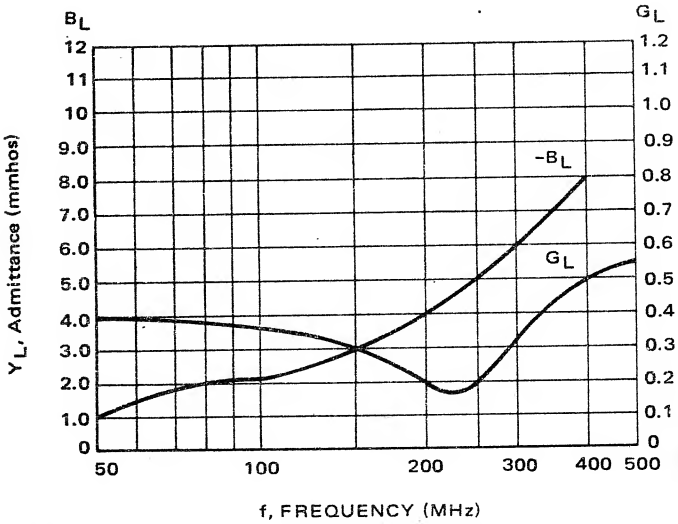
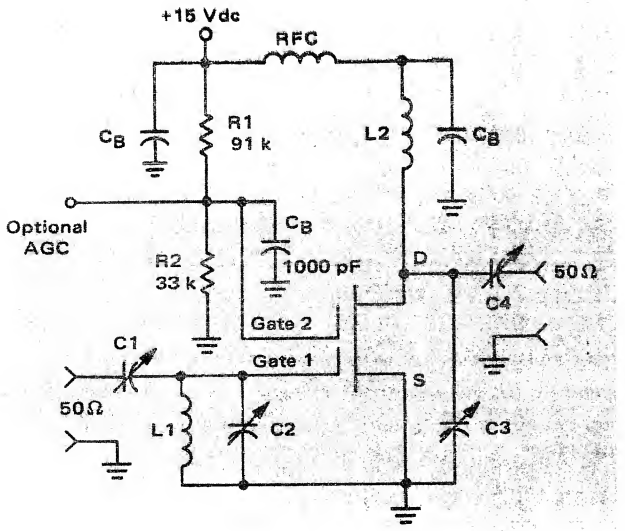


FIGURE 13 – Optimum Load Admittance, $Y_L = G_L + jB_L$ for Unneutralized G_T of Figure 11



Circuit Performance	100 MHz	200 MHz	400 MHz
Theoretical Power Gain from Figure 11	29 dB	22 dB	12.5 dB
Measured Power Gain	27.5 to 31.6 dB	21.2 to 24 dB	10.5 to 13.0 dB
Measured Bandwidth	3.5 to 5.5 MHz	4.0 to 5.2 MHz	11.0 to 15 MHz
Component Values			
C1	8.4 pF	4.6 pF	4.5 pF
C2	2.5 pF	6.0 pF	1.5 pF
C3	1.9 pF	1.0 pF	2.8 pF
C4	4.2 pF	2.0 pF	1.2 pF
L1	150 nH	42 nH	16 nH
L2	280 nH	110 nH	22 nH
CB	1000 pF	500 pF	250 pF

FIGURE 14 – VHF Amplifiers Using MFE3007

The parallel equivalent of this capacitance is needed for determining the bandwidth and resonance later in the design:

$$X'_{C4} = X_P = X_S \left[1 + \left(\frac{R_S}{X_S}\right)^2\right],$$

$$= 375 \left[1 + \left(\frac{50}{375}\right)^2\right]$$

$$= 382\ \Omega.$$

and the equivalent parallel capacitance is therefore

$$C4' = 4.2\ \text{pF}.$$

An equivalent circuit for the output tank after transformation of the load is shown in Figure 15B. Since the resistance across the output circuit is fixed by the parallel combination of R_{OUT} and R_L (after transformation) the desired bandwidth of the output tank will be determined by C3.

It should be noted that the output admittance (Y_{OUT}) of the device will not equal y_{os} under most conditions. Only when the input is terminated in a short circuit or the feedback admittance is zero does Y_{OUT} equal y_{os}. When y_{rs} is not zero, and the input is terminated with a practical source admittance, the true output admittance is found from the following:

$$Y_{OUT} = y_{os} - \frac{y_{rs}\, y_{is}}{y_{is} + Y_S}$$

$$= 0.04 + j1.7 - \frac{(10 - j5.5)(0 - j0.064)}{(0.15 + j3.0) + (1.3 - j4.4)}$$

$$= -0.055 + j2.05\ \text{mmhos}.$$

It should be noted that the value of Y_{rs} used (0 -j0.064) represents the composite feedback admittance of the device plus expected circuit strays. In this example a composite feedback capacitance of 0.1 pF has been used.

Therefore,

$$R_{OUT} = \frac{1}{G_{OUT}} = \frac{1}{-0.055 \times 10^{-3}} = -18.2\ \text{k}\Omega, \text{ and}$$

$$C_{OUT} = \frac{B_{OUT}}{2\pi f} = \frac{2.05 \times 10^{-3}}{2\pi \times 10^8} = 3.26\ \text{pF}.$$

The negative output impedance indicates the instability of the unloaded amplifier.

All other things remaining the same, oscillation will occur if the real part of the load impedance presented to the output tank of the amplifier is greater than 18.2 kΩ. This is of course due to the fact that the net real part of the output port impedance would be negative.

Now the total impedance across the output tank can be calculated:

$$R_T = \frac{1}{G_{OUT} + G_L}$$

$$= \frac{1}{-0.055 \times 10^{-3} + 0.35 \times 10^{-3}} = 3.39\ \text{k}\Omega$$

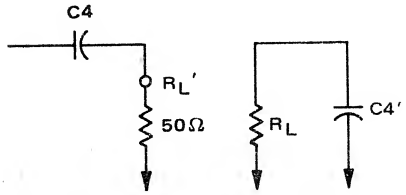


FIGURE 15A – Circuit Used for Output Impedance Transformation

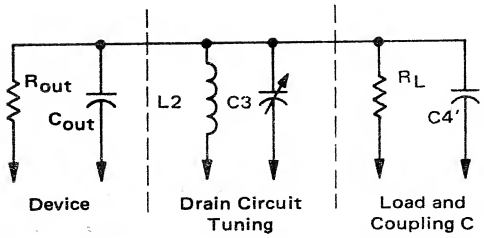


FIGURE 15B – Equivalent Output Circuit

Since the output impedance is several times higher than the input impedance of the device, amplifier bandwidth is primarily dependent upon output loaded Q. For a bandwidth of 5 MHz (3-dB points),

$$C_T = \frac{1}{2\pi R_T (BW)}$$

$$= \frac{1}{2\pi (3.39 \times 10^3)(5 \times 10^6)} = 9.4 \text{ pF}$$

hence

$$C3 = C_T - C_{OUT} - C4' = 9.4 - 3.26 - 4.2 = 1.9 \text{ pF}$$

The output inductance that resonates with C_T at 100 MHz is 269 nH. This completes the output circuit design.

Input calculations performed in a similar manner yield the following results:

$Y_S = 1.3 - j4.4$ mmhos.

$X_{C1} = 190\Omega$; therefore, C1 = 8.4 pF

$X'_{C1} = 203\Omega$; therefore, C1' = 7.8 pF

$$Y_{IN} = y_{is} - \frac{y_{fs}\, y_{rs}}{y_{os} + Y_L} = -0.23 + j4.25 \text{ mmhos; therefore,}$$

$R_{IN} = -4.35$ kΩ, $C_{IN} = 6.7$ pF.

$R_T = 935\ \Omega$.

The bandwidth of the input tuned circuit was chosen to be 10 MHz. Hence

$C_T = 17$ pF; therefore, L = 150 nH.

C2 = 17 - 6.7 - 7.8 = 2.5 pF

This completes the design of the tuned circuits. The results, plus those for similar 200-and 400-MHz amplifiers, are shown in Figure 14. To set the proper bias, resistors R1 and R2 are adjusted for 4 Vdc at gate 2. They have high values to minimize current drain. It is very important that gate 2 be well bypassed at the signal frequency as only a small impedance to ground may cause instability or loss in gain.

This 100-MHz amplifier was built and tested with different MFE3007's covering the I_{DSS} range. After tuning, all devices exhibited gains of 27.5 to 31.6 dB (theory predicted 29 dB), and bandwidths of 3.5 to 5.5 MHz (5-MHz design).

Similar amplifiers were designed, built and tested at 200 and 400 MHz. The component values and results are also shown in Figure 14.

NOISE FIGURE

An important consideration for many low-level amplifiers is noise figure. It is often necessary in bipolar designs to sacrifice power gain to obtain the optimum noise figure. Figure 16 shows the behavior of the noise figures and power gains of the MFE3007 versus source resistance at 100 MHz and 200 MHz. The dual-gate MOSFET offers two important advantages over most bipolar devices: very little, if any, power gain is sacrificed in achieving the best noise figure and both parameters are relatively independent of source resistance in the optimum region. These properties help alleviate the critical tuning and empirical adjustments usually required in front-end design. As a result, the designer has a great deal of flexibility in choosing a source impedance. In particular, it can be seen from Figure 16 that a 3:1 change in source resistance (300 ohms to 1000 ohms) results in only a 1-dB change in noise figure. If minimum cross modulation is a prime consideration, this 3:1 change in source resistance implies a 3:1 improvement in cross modulation and total harmonic distortion for the stage.

AUTOMATIC GAIN CONTROL

Most RF receivers have some means of controlling the overall receiver gain to accommodate a wide range of input signal levels. This is usually done by reducing the gain of the low-level RF and IF amplifier stages. Four different methods can be used to reduce the gain of the dual-gate MOSFET: (1) forward AGC (increasing voltage) at gate 1, (2) reverse AGC at gate 1, (3) forward AGC at gate 2, and (4) reverse AGC at gate 2. As will be shown, reverse AGC applied at gate 2 is superior to the other methods, but for completeness, each method will be discussed. Figure 3 shows y_{fs} as a function of the bias voltages at gates 1 and 2. As can be seen, y_{fs}, and therefore the gain, can be varied by changes in the bias voltage, on either gate. Three of the AGC methods reduce gain by lowering the transconductance between gate and drain. The fourth method of gain reduction, forward AGC at gate 2, reduces the output impedance of the device.

The maximum attenuation an unneutralized RF transistor (bipolar or FET) can achieve is limited by the feedback admittance (reverse transadmittance) of the device. Due to the very low C_{rss} of the dual-gate MOSFET, gain reductions greater than 50 dB are possible at 200 MHz. Because of the increasing reactance of the feedback capa-

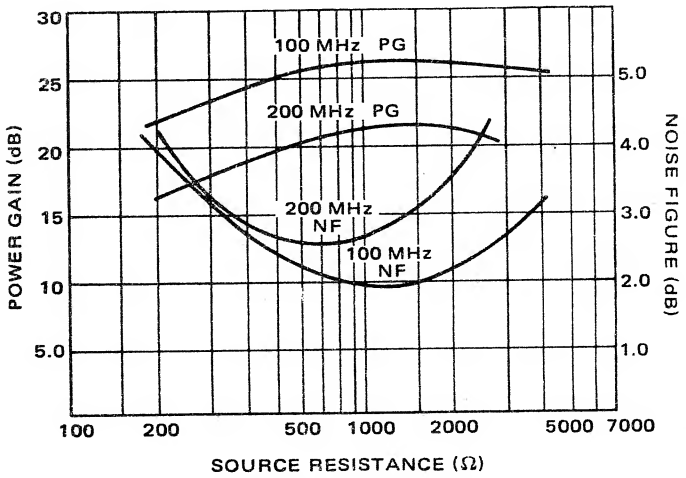


FIGURE 16 – Noise Figure (NF) and Power Gain (PG) of the MFE3007 at 100 and 200 MHz

citance with decreasing frequency, 85-dB gain reduction has been achieved in a 1-MHz amplifier.

AGC APPLIED AT GATE 1

With a constant gate-2 voltage, the transconductance can be reduced by varying the gate-1 voltage to either the left or the right of the peak-transconductance bias point indicated by the dashed line in Figure 3. The region to the left exhibits very rapid reduction in y_{fs} with decreasing bias between gate 1 and source. The sharp decrease in y_{fs} in this region is due to a rapidly approaching cutoff of that portion of the channel controlled by gate 1. This sharp cutoff introduces large third- and higher-order nonlinearities in the transadmittance at gain reductions greater than 10 dB. These nonlinearities induce distortion and degrade cross modulation and total harmonic distortion.

Forward AGC on gate 1 is a result of reduction in the transconductance when the bias point is shifted to the right of the dashed line in Figure 3 (the saturation region). Saturation results when the majority of the channel electrons adjacent to the gate have been ionized. Therefore, to modulate the conductivity, it is necessary to ionize the electrons farther from the gate. Since the capacitive charge-inducing capability of the gate is inversely proportional to distance, greater voltage changes are necessary for equivalent changes in conductivity, and therefore y_{fs} decreases. This method of AGC is limited to relatively small reductions due to excessive device dissipation at gain reductions greater than 10 dB. The increased device dissipation is due to the rapid increase in drain current with increasing forward bias on gate 1.

AGC APPLIED AT GATE 2

The best method of AGC is reduction of the gate-2 bias voltage from its initial optimum-gain bias point (greater than 4 Vdc). Application of the AGC signal to gate 2 results in a remote-cutoff characteristic (remote cutoff refers to a gradual reduction in I_d with decreasing gate bias). This type of I_d–V_G characteristic contrasts with the relatively abrupt cutoff of the drain current (and transconductance) when reverse AGC is applied to the gate of a single-gate MOS or junction FET. This sharp cutoff produces signal clipping, increasing distortion and cross modulation. Figure 17 shows the gain reduction when the AGC signal is applied to gate 2. The test circuit used for obtaining the gain-reduction curves is also shown. It is an unneutralized 100-MHz amplifier with a 3-MHz bandwidth. As the curves show, the initial gain-reduction rate is higher with a slight forward bias on gate 1 than for $V_{G1S} = 0$. This is due to the faster decrease in y_{fs} with decreasing V_{G2S} in the saturation region. This aspect of the gain-reduction rate may be useful in receiver designs where the RF AGC is delayed with respect to the IF to improve overall receiver distortion.

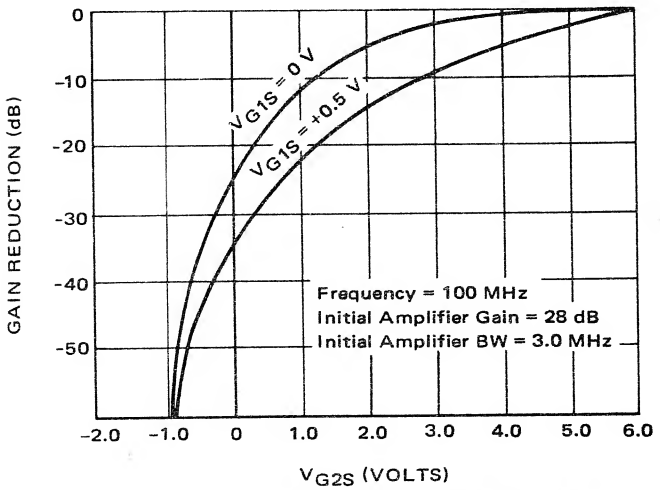


FIGURE 17 – Gain Reduction versus V_{G2S} (AGC Control)

The fourth method of gain reduction is by an increase in the dc bias voltage on gate 2. Unlike the previous methods cited, AGC in this manner is not the result of a reduction in y_{fs}. It can be said in fact, that any increase in V_{G2S} will always result in an increase in y_{fs} regardless of the bias point. The reduction in amplifier gain when forward AGC is applied to gate 2 is a result of the lower output impedance of the device as V_{G2S} approaches the supply voltage. This method is also limited to small gain reductions due to a limiting of the minimum value of the output impedance. The value of the output impedance at which this limiting occurs is about one order of magnitude less than the value at $V_{G2S} = 4$ V. Using the equation,

$$G_{max} = \frac{(y_{21})^2}{4(g_{11}g_{22})} = \frac{(y_{fs})^2}{4(g_{is}g_{os})},$$

a maximum gain reduction of approximately 10 dB can be obtained with this type of AGC. Another disadvantage of this method is the attendent increase in bandwidth when the output impedance of the device is reduced.

BANDWIDTH AND DETUNING

Forward AGC is usually used in bipolar amplifier designs when cross modulation and signal-handling capability are prime considerations. When this type of AGC is used, gain reduction is accompanied by a considerable increase in bandwidth and a shift in center frequency unless elaborate circuit techniques are employed. The increase in bandwidth is a result of the reduced output impedance of the bipolar device at high currents, while detuning is caused by the change in feedback and output capacitances as the output bias voltage is altered. When the AGC signal is applied to gate 2 of the dual-gate MOSFET, the output voltage, and therefore the C_{oss}, remains constant. The output impedance does increase slightly but the output circuit is usually loaded sufficiently that its effect on the bandwidth is small. In a 200-MHz amplifier with 5 MHz bandwidth (–3 dB points), 50-dB gain reduction was accompanied by only 1.25-MHz shift in center frequency and 0.75-MHz decrease in bandwidth.

DISTORTION CHARACTERISTICS

The most attractive feature of the field-effect transistor, at least to the RF designer, is its low distortion. The square-law transfer function of the field-effect transistor

results in a significant improvement in signal-handling capabilities and modulation and cross modulation distortion over that of bipolar transistors with their exponential transfer function. These transfer functions are shown in Figure 18. These characteristics are the products of theoretical first-order analyses and are usually inadequate for completely describing a practical device, but a qualitative comparison explains the low distortion of field-effect transistors:

The output current of a practical amplifier can be expressed in a power series about the operating point.

$$I_{OUT} = I_{dc} + \alpha V_g + \frac{\beta V_g^2}{2!} = + \frac{\gamma V_g^3}{3!} + \ldots \qquad (1)$$

where,

I_{dc} = dc bias current
V_g = input signal voltage at the gate
α = first derivative of transfer function (transconductance)
β = second derivative of transfer function
γ = third derivative of transfer function
(all derivatives evaluated at the dc bias point)

The second-and higher-order terms of this expansion account for signal distortion. Specifically, the second-order term ($\beta V_g^2/2!$) explains the sum and difference frequencies in a product mixer. Cross modulation, intermodulation, and modulation distortion are results of the third- and higher-odd-order curvature of the transfer characteristics.[2]

For the ideal linear amplifier, the second- and higher-order derivatives are zero, resulting in distortionless operation. On the other hand, practical amplifiers using both field-effect and bipolar transistors exhibit second-and higher-order curvature over the normal range of operation. However, due to the exponential nature of the transfer characteristic of bipolar transistors, distortion resulting from the third- and higher-order nonlinearities is usually much more severe in bipolar than in FET amplifiers. It is for this reason that most FM receivers are now being designed with field-effect transistors in their front ends.

SIGNAL-HANDLING CAPABILITY AND CROSS MODULATION

There are various methods of comparing the distortion characteristics of different devices. One of these methods is the overload or signal-handling capability of the device. Overload is frequently specified as the output signal level for one dB gain compression. This however represents a highly overloaded condition resulting in significant distortion of the input signal. For the signal-handling curves shown in Figure 19, overload is defined as the signal level at the input required to produce 5% total harmonic distortion in the output waveshape. The test setup is also shown in Figure 19. The test circuit was a 1-kHz common-source amplifier with the AGC signal applied at gate 2. The 1-kHz frequency was used instead of a modulated RF signal to eliminate the need for a detector in the test setup.

The signal-handling capability is a function of the gain reduction and is therefore usually plotted as such for transistors designed for automatic gain control. This dependence is due to the changing analytic character of the transfer function as the bias point is altered during AGC. When constant gate-1 bias load lines are drawn through the curves of Figure 3, the order of the curvature chiefly responsible for the distortion can be seen. For zero bias between gate 1 to source, the reduced signal-handling capability at the 15-dB gain-reduction level is due to the high third-order curvature of the transfer characteristic in that region. For V_{G1S} = 0.55 V, increasing distortion is due mainly to second-order distortion in the 5-to-20-dB gain-reduction portion of the curves. For any load line, an increase in gain reduction reduces the transconductance, which contributes to an increase in distortion.

Another distortion curve often needed to evaluate the performance of RF amplifiers is the cross-modulation characteristics. Cross modulation is the transfer of modulation from one RF signal to another, when both signals

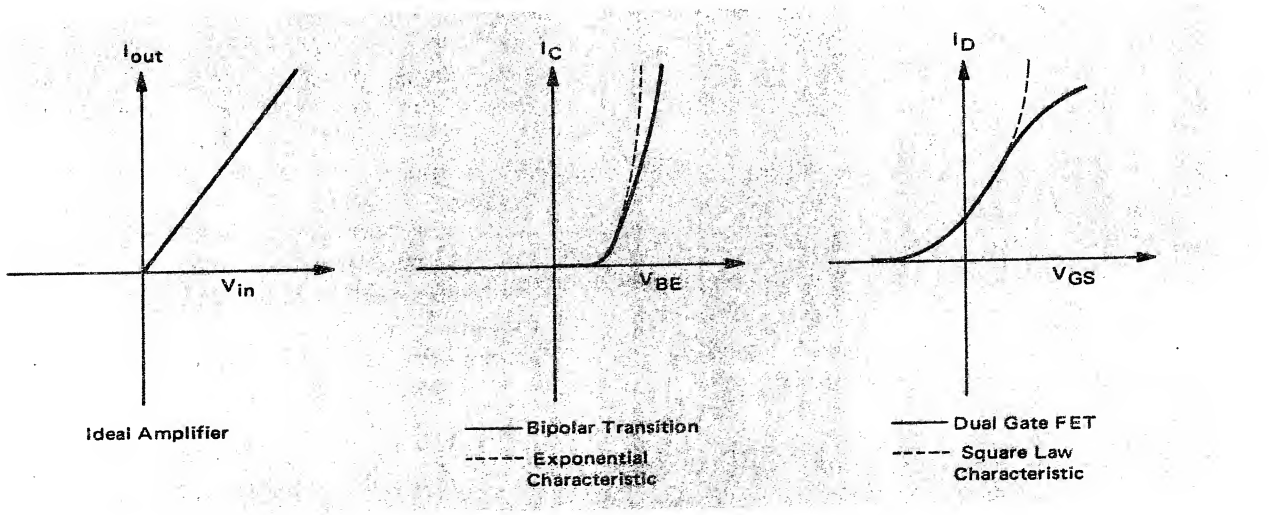


FIGURE 18 – Transfer Characteristics of Amplifiers

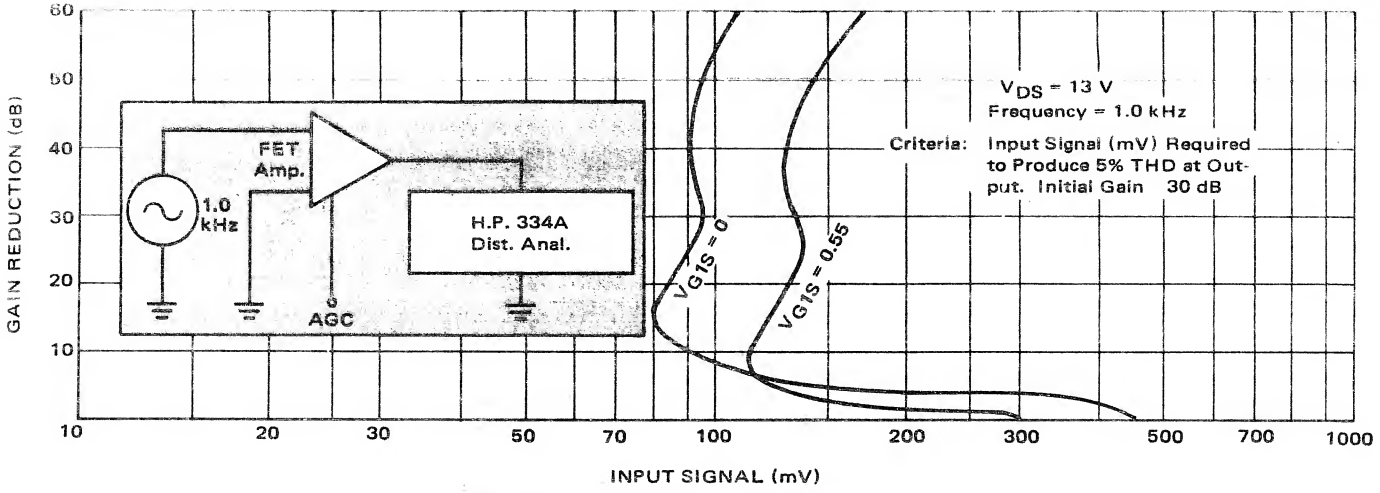


FIGURE 19 — Signal-Handling Capability

are present at the input of an amplifier. The precise definition for the cross-modulation index plotted in Figure 20 is the level of undesired signal necessary to transfer 0.03% modulation to the desired signal when the undesired signal is modulated 30% at 1 kHz. The frequencies of the desired and undesired signals are 200 MHz and 150 MHz. For meaningful results the input to the amplifier should provide no selectivity and the desired signal level should not overload the amplifier. Measurements were made for two different V_{G1S}-bias conditions. As the curves show, forward bias on gate 1 significantly improves cross-modulation performance.

MIXER OPERATION

Two basic methods of local-oscillator injection can be used with a MOSFET mixer. One uses gate 1 for both the local-oscillator and signal injection. The second uses gate 1 for signal injection with the local oscillator applied to gate 2. A third possibility, local-oscillator injection at the source acts as a particular case of the first method and will not be discussed further. Both methods of injection have been investigated and will be discussed briefly.

LOCAL OSCILLATOR INJECTION AT GATE 1

When both the signal and local-oscillator are injected at gate 1, optimum mixer performance will occur with a particular gate-1-to-source bias. The reason for this becomes evident when one examines the mechanism of the conversion process for this type of mixer operation. When the sum of two cosinusoidal signals is substituted for V_g in Equation (1), the power expansion previously presented, the second-order term $\beta(V_2)^2/2!$, is seen to produce the desired sum and difference products. More specifically, the difference term is

$$i_{S\text{-}LO} = \frac{\beta}{2} V_S V_{LO} \cos(\omega_S - \omega_{LO})t \qquad (2)$$

the conversion transconductance, usually denoted g_C, is defined as

$$g_C = \frac{i_{S\text{-}LO}}{V_S} = \frac{\beta}{2} V_{LO} \text{ mhos} \qquad (3)$$

where spurious responses (i.e., frequencies in the output other than those desired) are obtained when a similar pro-

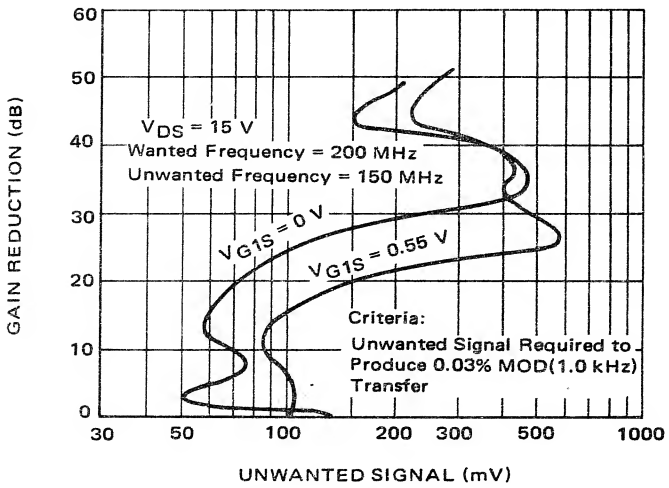


FIGURE 20 — Cross Modulation Curves

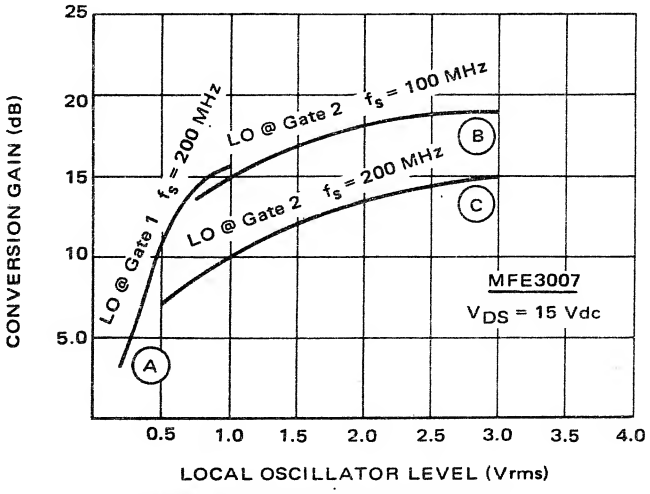


FIGURE 21 — Conversion Power Gain versus Local Oscillator Injections

cedure is carried out for the third- and higher-order terms.

In selecting a bias point, then, two things should be kept in mind: high g_C, and good linearity. A large g_C requires either a high β or a large peak-to-peak local oscillator voltage or both. With these considerations in mind an examination of Figure 3 shows that a bias of $V_{G1S} = -0.5$, $V_{G2S} = 4$ V yields an optimum β for a large peak-to-peak local-oscillator voltage. By Equation (3) the conversion gain for a straight-line approximation of y_{fs} between V_{G1S}'s of 0 V and −1 V, is seen to be:

$$g_C = \frac{12 - 2.5}{2} V_{LO} = 4.75\ V_{LO}\ \text{(Peak Volts)}$$

$$= 6.65\ V_{LO}\ \text{(rms) mmhos}$$

Figure 21 shows conversion gain versus local-oscillator injection voltage when the local-oscillator is applied to gate 1 (Curve A). Test conditions for the mixer curve are signal frequency of 200 MHz, local-oscillator frequency of 230 MHz, IF frequency of 30 MHz, V_{DS} of 15 Vdc, V_{G1S} of 0.5 Vdc, and V_{G2S} of 4 Vdc (ac bypassed to ground). As can be seen, the conversion gain reaches a maximum of 15 dB for an local-oscillator voltage of approximately 1 Vrms. For a local-oscillator injection in excess of 1 V (rms), the device begins to saturate on the positive peaks of the local-oscillator voltage. In addition to limiting the conversion gain, this clipping action also increases spurious responses.

LOCAL-OSCILLATOR INJECTION AT GATE 2

When the local oscillator is applied to gate 2, somewhat higher injection levels are required for conversion gains comparable to the previous method. The reason for this is the lower gate-to-drain transconductance of gate 2. However, this type of injection may serve well in mixer applications where it is desirable to isolate the local oscillator from both the input and output networks. Figure 21 also shows conversion gain versus local oscillator injection for this method of local oscillator injection for mixers with signal input frequencies of 100 MHz (Curve B) and 200 MHz (Curve C). The local oscillator frequencies were 130 MHz and 230 MHz, and in both cases the 30-MHz difference frequency serves as the IF. The test conditions for both mixers were $V_{DS} = 15$ V, V_{G1S} and $V_{G2S} = 0.3$ V to 0.5 V.

SUMMARY

In summary, the dual-gate MOSFET should be considered for small-signal RF applications where signal-handling and distortion characteristics are important. It is especially attractive in low-level amplifiers where AGC is used. This application note has included data for the MFE3007 that permits rapid evaluation and design of low-level RF amplifiers in the 10-to 500-MHz range.

REFERENCES

1. "Field-Effect Transistors in Theory and Practice," Motorola Application Note AN-211.
2. "RF Small-Signal Design Using Two-Port Parameters," Motorola Application Note AN-215.
3. "Field-Effect Transistor RF Amplifier Design Techniques," Motorola Application Note AN-423.
4. "UHF Amplifier Design Using Data Sheet Design Curves," Motorola Application Note AN-419.
5. Deketh, j., Fundamentals of Radio Valve Techniques, N. V. Philips Gloeilampenfabricken, Eindhoven, Netherlands, 1949.

MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

4597-3 PRINTED IN USA 11-71 IMPERIAL LITHO 825832 10M

AN 478A